

## **Title: Network-on-Chip: The Next Generation of Multi-Processor System-on-Chip**

**Duration:** Half Day (4 hrs)

### **Description of Tutorial:**

Multi-Processor System-on-Chip (MPSoC) has been a landmark in the evolution of parallel processing for high performance computation. Modern computers and laptops consist of dual cores, quad cores, and even six cores. The communication backbone of these cores is bus based. Upto 8 cores in a single chip, the performance of these bus-based SoCs are satisfactory; however, scalability degrades with more number of cores due to communication bottleneck. On-chip interconnection network is one solution to integrate cores in complex SoCs. Usage of Network-on-Chip (NoC) in SoC design is an evolution of bus interconnects technology. In recent years, NoC has become a broad topic of research encompassing the design of hardware communication structure, CAD flows to design application specific NoC, testing, and so on. In this tutorial, we are mainly focusing on architecture design, power-performance-reliability trade-off, and application mapping in NoC.

In NoC, various intellectual property (IP) cores are connected to the communication fabric (router-based network) using Network Interfaces (NIs). Due to the frequency mismatch of IP cores and routers, Globally Asynchronous and Locally Synchronous (GALS) style of communication is required through mixed clock FIFO (separate clocks for reading and writing). The network is used for packet switched on-chip communication among cores. The performance of the network depends on the topology selection and routing algorithm. The routing algorithm should be deadlock and live-lock free. The tutorial focuses on the architectural issues, like switching techniques, topology selection, routing, buffering, arbitration, flow control protocol, and GALS implementation, in detail. It also highlights on the detailed architecture design of on-chip router as well as the traffic generation and simulation methodology for evaluating performance and power estimation of the entire network. The comparison between different commonly used network topologies, in terms of throughput, bandwidth, latency, area, and power consumption will also be taken out.

Once a topology has been decided to implement an application consisting of a set of concurrent tasks, the most important part is the mapping of the tasks onto the network. The tasks are assumed to have been scheduled on a list of selected IP cores. The mapping problem is to decide how to topologically place the selected cores, so that the application will meet the bandwidth requirements. This definitely affects both the performance and energy consumption of the NoC. The tutorial will give a detailed view of application mapping onto the network.

The major challenge in NoC design in deep sub-micron (DSM) era, where almost 80% of system failures are associated with transient faults, is reliability in communication. In NoC, the on-chip routers communicate with each other via point-to-point interconnection links. With shrinking feature size, increasing interconnection density, and decreasing inter-wire spacing, capacitive crosstalk is a major source of transient error in NoC interconnects. With decreasing supply voltage for low power design, a significantly lower charge deposited by a particle strike (known as soft errors) suffices to flip the logic value of a node, thus creating a transient pulse. Power supply noise and electromagnetic interference (EMI) are other two sources of transient faults in any VLSI circuit. The tutorial focuses on the fault tolerant schemes employed in NoC design, such as, detection and retransmission, error correction, and hybrid scheme, to handle with the transient faults.

The FIFO consumes almost 75% percent power of the router. Reducing FIFO depth for minimizing power will cause performance degradation. So there must be a trade-off between power and performance in terms of buffer depth. Supply voltage ( $V_{DD}$ ), the most dominant component, has quadratic impact on dynamic power dissipation. Unfortunately, this reduction in power dissipation comes at the expense of performance and reliability. Dynamic voltage scaling is normally adopted to minimize power when the network link is under-utilized. The tutorial focuses on the power-performance and power-reliability trade-off in NoC due to supply voltage scaling. We will also focus on multi-level voltage and dynamic frequency scaling approaches in detail and NoC design in 3D environment for achieving better performance together with power reduction.

### **Brief Profile of Authors:**



**Santanu Kundu** received his B.Tech in Instrumentation Engineering from Haldia Institute of Technology, Vidyasagar University, West Bengal in 2002 and M.Tech in Instrumentation and Electronics Engineering from Jadavpur University, West Bengal in 2006. Currently, he is pursuing PhD in Electronics and Electrical Communication Engineering from Indian Institute of Technology, Kharagpur. His research interest includes Network-on-Chip architecture design and power-performance-reliability trade-off.



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